IN THE CLAIMS

1.-16. (canceled)

17. (previously presented): ~~The semiconductor device according to claim 16,~~

A semiconductor device, comprising:

a semiconductor substrate which includes a first region that includes a plurality of circuit element connection pads, and a second region that surrounds the first region;

a plurality of first external terminals which are arranged over the first region;

a plurality of second external terminals which are arranged over the second region;

a plurality of first wiring structures which are formed over the first region, and electrically and individually connect a plurality of the first external terminals and a first predetermined number of the circuit element connection pads;

a plurality of second wiring structures which are formed from the first region to the second region, and electrically and individually connect a plurality of the second external terminals and a second predetermined number of the circuit element connection pads;

a passive element which is disposed over the second region, and which is electrically connected to one of the second wiring structures; wherein;

each of the first wiring structures includes a first redistribution wiring layer which is electrically and individually connected to one of the first predetermined number of the circuit element connection pads, and a first post electrode which electrically and individually connects the first redistribution wiring layer and the one of the first external terminals;

each of the second wiring structures includes a second redistribution wiring layer which is formed ranging from the first region to the second region and is electrically and individually connected to one of the circuit element connection pads, and a second post electrode which electrically and individually connects the second redistribution wiring layer and one of the second external terminals; and

the passive element is electrically connected to one of the second redistribution wiring layer; and wherein;

the passive element is a capacitor which includes an upper electrode, a lower electrode and a dielectric film which is placed between the upper electrode and the lower electrode; and

the upper electrode is electrically connected to one of the second redistribution wiring layer, and the lower electrode is electrically connected to another of the second redistribution wiring layer.

18. (currently amended): The semiconductor device according to claim [[16,]] 17, wherein the passive element is an inductor which is placed in a route of the second redistribution wiring layer.

19. (canceled)

20. (currently amended): ~~The semiconductor device according to claim 19,~~

A semiconductor device, comprising:

a semiconductor substrate which includes a first region that includes a plurality of circuit element connection pads, and a second region that surrounds the first region;

a plurality of first external terminals which are arranged over the first region;

a plurality of second external terminals which are arranged over the second region;

a plurality of first wiring structures which are formed over the first region, and electrically and individually connect a plurality of the first external terminals and a first predetermined number of the circuit element connection pads;

a plurality of second wiring structures which are formed from the first region to the second region, and electrically and individually connect a plurality of the second external terminals and a second predetermined number of the circuit element connection pads;

a passive element which is disposed over the second region, and which is electrically connected to one of the second wiring structures; wherein;

each of the first wiring structures includes a first redistribution wiring layer which is electrically and individually connected to one of the first predetermined number of the circuit element connection pads, and a first post electrode which electrically and individually connects the first redistribution wiring layer and the one of the first external terminals;

each of the second wiring structures includes a second redistribution wiring layer which is formed from the first region to the second region and is electrically and individually connected to one of the circuit element connection pads, and a second post electrode which electrically and individually connects the second redistribution wiring layer and one of the second external terminals; and

the passive element is electrically connected to one of the second redistribution wiring layer via a passive element electrode pad which is placed over the second region; wherein;

the passive element is a capacitor which includes an upper electrode, a lower electrode and a dielectric film which is placed between the upper electrode and the lower electrode;

a first capacitor connection pad which is a passive element electrode pad being electrically connected to the upper electrode, and a second capacitor connection pad which is a passive element electrode pad being electrically connected to the lower electrode are comprised; and

the first capacitor connection pad is electrically connected to one of the second redistribution wiring layer, and the second capacitor connection pad is electrically connected to another of the second redistribution wiring layer.

21. (currently amended): The semiconductor device according to claim [[19,]] 20, wherein;

the passive element is an inductor,

two passive element electrode pads are electrically connected to one passive element, in which these two passive element electrode pads are first and second inductor connection pads; and

the first and second inductor connection pads are electrically connected to corresponding second redistribution wiring layer respectively.

22. (currently amended): The semiconductor device according to claim [[19,]] 20, wherein a plurality of the passive elements are arranged in the shape of an array.

23. (canceled)